(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 504 875 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92104781.7**

(51) Int. Cl.5: **H01L 29/73**, H01L 21/331

(22) Date of filing: **19.03.92**

(30) Priority: **20.03.91 JP 57090/91**

(43) Date of publication of application:
23.09.92 Bulletin 92/39

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **HITACHI, LTD.**
6, Kanda Surugadai 4-chome
Chiyoda-ku, Tokyo 101(JP)

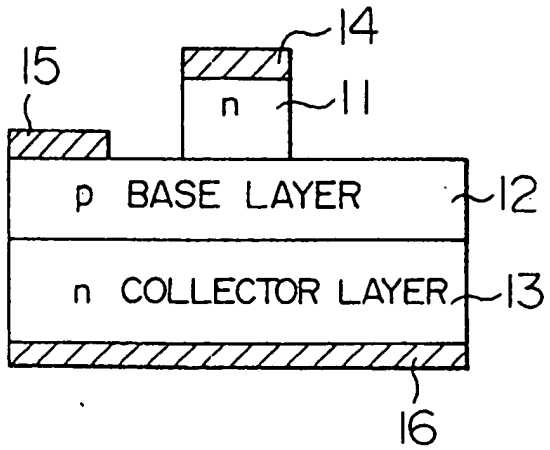
(72) Inventor: **Shoji, Kenichi**
Hitachi Daiyon Kyoshinryo A201, 14-6
Nishikoigakubo-4-chome, Kokubunji-shi(JP)
Inventor: **Fukami, Akira**
Hitachi Suzuki Shinden Shataku A3-2
16-3-2, Josuihoncho-5-chome,
Kodaira-shi(JP)
Inventor: **Nagano, Takahiro**
10-10, Kanesawacho-7-chome
Hitachi-shi(JP)

(74) Representative: **Patentanwälte Beetz - Timpe - Siegfried - Schmitt-Fumian- Mayr**
Steinsdorfstrasse 10
W-8000 München 22(DE)

(54) Bipolar transistor and method of fabricating the same.

(57) To eliminate misfit dislocation occurring in a hetero-interface and to provide a bipolar transistor capable of a high speed operation, the bipolar transistor is configured such that the energy band gap is progressively narrowing from part of an emitter layer (11) towards part of a collector layer (13) through a base layer (12).

FIG. 1A



EP 0 504 875 A2

BACKGROUND OF THE INVENTION

The present invention relates to a bipolar transistor, and more particularly to a heterojunction bipolar transistor and a fabrication method thereof.

When the delay time of a basic gate is compared in terms of a trend in a highly integrated memory of each generation, performance of a bipolar transistor must be improved in the same way as an MOS transistor in order to keep superiority of a BiCOMS gate over a CMOS gate in future. When the switching time is compared between the MOS transistor and the bipolar transistor that are used in the BiCMOS gate circuit, the switching speed of the bipolar transistor tends to decrease in the silicon system of the prior art although a high speed switching time can be accomplished in the MOS transistor with the scale-down of the transistor size and its lowering voltage.

One of the high speed bipolar transistors is a heterojunction bipolar transistor which has a difference of the band gap between its base region and emitter region. The characterizing feature of the heterojunction bipolar transistor is that a high current gain can be obtained by preventing the injection of majority carriers from the base region to the emitter region by utilizing the barrier height of the step of the band gap on the hetero-interface of the emitter-base junction. In consequence, since the base concentration can be set to a relatively higher concentration than in the conventional bipolar transistors, the base resistance can be reduced and higher speed performance of the bipolar transistor can be accomplished.

The structure of the conventional heterojunction bipolar transistor uses a silicon-germanium alloy ($Si_{1-x}Ge_x$) for its base region, and Fig. 19 shows its sectional view. Reference numeral 2 in the drawing represents an n^+-Si collector region, 3 is a p-$Si_{1-x}Ge_x$ base region, 4 is n^+-Si emitter region, 5 is an emitter electrode, 6 is a base electrode and 7 is a collector electrode. Among them, the X value of $Si_{1-x}Ge_x$ in the base region is increased from the emitter region side towards the collector region side and the energy band gap becomes narrower from the emitter region side towards the collector region side. Therefore, a drift field is generated in the base region, so that the base transit time of the minority carriers can be shortened and high speed performance of the bipolar transistor can thus be accomplished.

A heterojunction bipolar transistor using the silicon-germanium alloy ($Si_{1-x}Ge_x$) for the base is described, for example, in JP-A-1-231371.

According to the prior art described above, since the band gap of the emitter and base regions sharply changes at the emitter-base junction, misfit dislocations resulting from the lattice mismatch between silicon and germanium occur in the active regions of the bipolar transistor and the problems such as the drop of high speed performance and breakdown voltage of the bipolar transistor and the increase of the leakage current are caused.

Generally, in hetero-epitaxy of lattice mismatched materials such as silicon and germanium, a growth layer coherently grows without generating misfit dislocations and the lattice mismatch is mitigated by a strain in the lattice when a film thickness is below a thickness approximate to a superlattice, but when the growth layer grows into a thickness about the film thickness necessary for constituting the bipolar transistor, the lattice mismatch invites the strain in the lattice and the misfit dislocations. The occurrence of the misfit dislocations which exerts adverse influences on the electrical characteristics is a critical problem which is unavoidable when a hetero-material of the silicon-germanium alloy ($Si_{1-x}Ge_x$) is injected into the Si system bipolar transistor.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a bipolar transistor minimizing the influences of the misfit dislocations which occur when the hetero-junction is formed, and a fabrication method suitable for the bipolar transistor.

The characterizing structure of the bipolar transistor of according to one feature of the present invention resides in that an energy band gap in the emitter and base regions near a base-emitter junction is narrowing from the emitter region side towards the base region side.

Definitely speaking, the characterizing structure of the bipolar transistor of according to another feature of the present invention is as follows. The emitter region and the base region near the base-emitter junction include an alloy of silicon and germanium, and the concentration of germanium progressively increases from the emitter region side towards the base region side. The silicon-germanium alloy region is preferably disposed in a spaced-apart relation from an exposed end of the base-emitter junction. Further preferably, at least the alloy region contains an element or elements having a smaller lattice constant than silicon, such as the element(s) selected from the group essentially consisting of carbon, boron and nitrogen.

The characterizing feature of the fabrication method of a bipolar transistor according to another feature of the present invention comprises a first step of preparing a silicon substrate having a region to serve as a base of the transistor and a region to serve as a collector of the transistor that are sequentially formed on one of main surfaces of the silicon substrate, a second step of forming a

mask having a window on one main surface of the silicon substrate, and forming a silicon-germanium alloy region in which the germanium concentration increases progressively away from one main surface of the substrate inside the region to serve as the base by injecting germanium into at least the region to serve as the base from the window of the mask, and a third step of injecting an impurity from the window of the mask to form a region to serve as an emitter of the transistor so that the base-emitter junction is positioned in the silicon-germanium alloy region. Preferably, this fabrication method includes also a step of making the window of the mask in the third step greater than the window of the mask in the second step and injecting an element or elements having a smaller lattice constant than that of silicon into the region to serve as the emitter.

The bipolar transistor according to one feature of the invention has a structure in which the energy band gap decreases progressively from the emitter region side towards the base region side. Therefore, the generation of the misfit dislocations at the emitter-base junction can be prevented and the problems with the prior art, that is, degradation of the electrical characteristics in the hetero-interface or in other words, the drop of high speed performance and the increase of the leakage current, can be eliminated, so that high-speed performance of the bipolar transistor can be improved. Since the band gap inside the base is changed, too, the high speed performance of the bipolar transistor can further be promoted by the effective drift field in the base region.

Since carbon (C) having a function of widening the band gap is injected into the emitter region side, the barrier height of the valence band at the emitter-base junction becomes great, so that the current gain is improved and the high speed performance of the bipolar transistor is enhanced. The same effect can be obtained by injecting two elements having a smaller lattice constant than that of silicon as when carbon (C) is injected.

From the aspect of the structure, the bipolar transistor according to the present invention keeps the emitter-base junction away from the misfit dislocations occurring on the surface of the silicon-germanium alloy region by making the area of the emitter region on the substrate surface greater than the area of the silicon-germanium alloy ($Si_{1-x}Ge_x$) region, and can limit the degradation of the electrical characteristics of the bipolar transistor due to the misfit dislocations.

Since carbon (C) is an element of the Group IV in the same way as silicon and germanium, is electrically intrinsic and has a lattice constant smaller than that of silicon, the injection of carbon into the substrate surface provides the effect of suppressing the occurrence of the misfit dislocations on the surface of the silicon-germanium alloy region by mitigating the strain resulting from the lattice mismatch between silicon and germanium.

The injection of two elements having a smaller lattice constant than that of silicon into the substrate surface provides a greater suppression effect of the misfit dislocations than the injection of carbon because the two elements (such as boron (B) and nitrogen (N)) having ion bondability make reconstruction of the silicon-germanium alloy easier than carbon (C) which is a covalent bondable element having high bonding power.

Widening of the width of the substrate surface layer in the base region in a silicon-germanium alloy base lateral hetero-junction bipolar transistor keeps the emitter-base junction as well as the base-collector junction away from the misfit dislocations, suppresses the occurrence of any excessive current at the emitter-base junction and reduces the occurrence of the leakage current at the base-collector junction.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1E are conceptual views of a bipolar transistor according to an embodiment of the present invention, a germanium concentration distribution diagram and an energy band diagram.

Figs. 2A-2B are a concentration distribution diagram of a bipolar transistor as a modification of the first embodiment and its energy band diagram.

Figs. 3A-3B are a concentration distribution diagram of a bipolar transistor as another modification of the first embodiment and its energy band diagram.

Figs. 4A-4B are a plan view and a sectional view of a bipolar transistor according to another embodiment of the present invention.

Figs. 5A-5D are fabrication process diagrams of the bipolar transistor of Fig. 4.

Figs. 6A-6B are a plan view and a sectional view of a bipolar transistor as a modification of the embodiment of Fig. 4.

Figs. 7A-7D are fabrication process diagrams of the bipolar transistor of Fig. 6.

Figs. 8A-8D are fabrication process diagrams of a bipolar transistor as another modification of the embodiment of Fig. 4.

Figs. 9A-9D are fabrication process diagrams of a bipolar transistor as a further different modification of the embodiment of Fig. 4.

Figs. 10A-10D are fabrication process diagrams of a bipolar transistor as still another modified embodiment of the embodiment of Fig. 4.

Figs. 11A-11D are fabrication process diagrams of a bipolar transistor as still another modified embodiment of the embodiment of Fig. 4.

Figs. 12A-12D are fabrication process diagrams of a bipolar transistor according to still another embodiment of the present invention.

Figs. 13A-13B are a plan view and a sectional view of a bipolar transistor according to still another embodiment of the present invention.

Figs. 14A-14D are fabrication process diagrams of the bipolar transistor of Fig. 13.

Figs. 15A-15B are a BiCMOS basic gate (2NAND) circuit diagram using the bipolar transistor according to the present invention and a sectional view of a cell.

Fig. 16 is a circuit diagram for a two-input NOR of an ECL (using only the NOR side output) gate array using the bipolar transistor according to the present invention.

Figs. 17A-17B are a circuit diagram of a clamp type memory cell using the bipolar transistor according to the present invention and a sectional view of a memory cell.

Fig. 18 is a plan view of a microprocessor to which the bipolar transistor according to the present invention is applied.

Fig. 19 is a schematic view of a heretofore known bipolar transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, embodiments of the present invention will be explained with reference to the accompanying drawings. Although the explanation will be given about an NPN bipolar transistor only by way of example for the purpose of simplification, it also holds true of a PNP transistor.

Figs. 1A-1E show an embodiment of the bipolar transistor of the present invention. Fig. 1A is a conceptual view of the bipolar transistor, Fig. 1B shows a concentration distribution of germanium (Ge) inside silicon (Si), Fig. 1C is an energy band diagram under a flat band state before a junction is formed, Fig. 1D shows the state of the energy band before an impressed voltage is applied, and Fig. 1E shows the state of the energy band when the impressed voltage is applied. It is possible to eliminate the occurrence of a misfit dislocation at an emitter-base junction and to let the bipolar transistor in this embodiment fully exhibit its high speed performance by progressively narrowing the band gap from part of an emitter region 11 to part of a collector region 13 through a base region 12 as shown in Fig. 1C. In Fig. 1A, reference numeral 14 denotes an emitter electrode, 15 is a base electrode and 16 is a collector electrode.

Figs. 2A-2B show a bipolar transistor as a modification of the embodiment shown in Figs. 1A-1E. Fig. 2A shows a concentration distribution of germanium (Ge) and carbon (C) inside silicon (Si), and Fig 2B shows the state of the energy band before the impressed voltage is applied. A bipolar transistor having a high current gain and capable of a high speed operation can be accomplished by thus doping carbon (C) into the emitter region and increasing much more the barrier height of a valence band near the emitter-base junction.

Figs. 3A-3B show a bipolar transistor as another modification of the embodiment shown in Figs. 1A-1E. Fig. 3A shows a concentration distribution of germanium (Ge), boron (B) and nitrogen (N) inside silicon (Si), and Fig. 3B shows the state of the energy band before the impressed voltage is applied. A bipolar transistor having a high current gain and capable of a high speed operation can be accomplished by thus doping boron (B) and nitrogen (N) having a smaller atomic radius than silicon (Si) into the emitter and increasing much more the barrier height of the valence band near the emitter-base junction.

Embodiment 2:

Figs. 4A-4B show a structure of a bipolar transistor according to another embodiment of the present invention.

Fig. 4A is a plan view and Fig. 4B is a sectional view. The characteristic feature of the present bipolar transistor resides in the structure wherein an emitter region 21 encompasses the surface layer of a silicon-germanium alloy ($Si_{1-x}Ge_x$) region 24 locally formed inside a base region 22 and the emitter region 21. Since the base-emitter junction is spaced apart from the silicon-germanium alloy region 24 in which misfit dislocation is likely to occur, on the main plane, the structure prevents degradation of electrical characteristics of the bipolar transistor resulting from the misfit dislocation. Reference numeral 23 represents a collector region, 25 is the emitter electrode, 26 is a base electrode, 27 is a collector electrode, 28 is a field oxide film, 291 is an oxide film for inter-level insulation, and 292 is a surface stabilization film.

Figs. 5A-5D show a fabrication process of the bipolar transistor shown in Figs. 4A-4B.

In Fig. 5A, an n^+-buried layer 231 and an n-collector 232 are formed on an Si substrate 20, and a field oxide film 28 is formed on field regions of the bipolar transistor. A P-type base region 221 is formed on one of the sides and an n^+-collector plug 233, on the other side. In Fig. 5B, after the oxide film 291 is formed, its predetermined region is opened and germanium ion implantation is carried out. In this instance, ion implantation is preferably carried out while cooling an Si substrate to a low temperature (below 0°C). In Fig. 5C, after a base extension region 222 to the outside is formed

and a window of the oxide film 291 is widened, polycrystalline silicon 251 is deposited and arsenic is ion-implanted for doping an emitter region. Polycrystalline silicon 251 is etched in such a manner as to cover the window. In Fig. 5D, after the surface stabilization film 292 is deposited, annealing is carried out so as to activate the implanted ions and to shallowly diffuse arsenic in polycrystalline silicon into the base region 221. Finally, predetermined regions of the oxide film 291 for inter-level insulation and surface stabilization film 292 are opened and an emitter electrode 252 is formed on polycrystalline silicon 251, furthermore, the base electrode 26 is formed on an external base extension region 222 and a collector electrode 27 is formed on the collector plug 233.

Figs. 6A-6B show a structure of the bipolar transistor as a modification of the embodiment shown in Figs. 4A-4B. Fig. 6A is a plan view and Fig. 6B is a sectional view. In comparison with Figs. 4A-4B, the characterizing feature of this embodiment resides in that the silicon-germanium alloy ($Si_{1-x}Ge_x$) region 24 reaches the n^--collector layer 232 of the collector region 23. Since the silicon-germanium alloy ($Si_{1-x}Ge_x$) region 24 expands up to the base region 22 and to the collector region 23, a sharp hetero-interface does not exist at the base-collector junction; hence, the reduction of the leakage current in the opposite direction can be accomplished.

Figs. 7A-7D show a fabrication process of the bipolar transistor shown in Figs. 6A-6B.

In Fig. 7A, the n^+-buried layer 231 and the n^--collector layer 232 are formed on the Si substrate 20, and the field oxide film 28 is formed on the field regions of the bipolar transistor. The p-base layer 22 and the collector plug n^+-region 233 are formed at the portions where the field oxide film 28 does not exist. In Fig. 7B, the oxide film 291 is formed and its predetermined region is opened. Then, ion implantation of the germanium ion is carried out. At this time, ion implantation is carried out so that the germanium ion can be injected into the n^--collector layer 232. In Fig. 7C, after the base extension region 222 to the outside is formed and the window of the oxide film 291 is widened, polycrystalline silicon 251 is deposited, and arsenic is ion-implanted for doping the emitter region. Polycrystalline silicon 251 is etched in such a manner as to cover the window. In Fig. 7D, after the surface stabilization film 292 is deposited, annealing is carried out in order to activate the ions and to shallowly diffuse arsenic in polycrystalline silicon into the base region 221. Finally, the predetermined regions of the oxide film 291 for inter-level insulation and the surface stabilization film 292 are opened and the emitter electrode 252 is formed on polycrystalline silicon 251. Furthermore, the base electrode 26 is formed on the external base extension region 222 and the collector electrode 27 is formed on the collector plug 233.

Figs. 8A-8D show a structure of the bipolar transistor as still another modification of the embodiment shown in Figs. 4A-4B and its fabrication process. The bipolar transistor according to this modification is featured in that carbon (C) is doped into the emitter region 21 and the surface of the silicon-germanium ($Si_{1-x}Ge_x$) alloy region 24. The strain in the lattice resulting from the lattice mismatch between silicon and germanium can be mitigated by introducing carbon (C) having a smaller lattice constant than silicon, so that the density of the misfit dislocation occurring in the surface layer of the silicon-germanium alloy ($Si_{1-x}Ge_x$) is reduced and the electrical characteristics at the junction between polycrystalline silicon 251 and the emitter region 21 can be improved.

In Fig. 8A, the n^+-buried layer 231 and the n^--collector layer 232 are formed on the Si substrate 20 and the field oxide film 28 is formed on the field regions of the bipolar transistor. The p-base layer 221 is formed on one of the sides and the n^+-collector plug 233 is formed on the other side. In Fig. 8B, after the oxide film 291 is formed and its predetermined region is opened, germanium is ion-implanted. Further, carbon (C) for mitigating the crystal strain is ion-implanted. In Fig. 8C, after external base extension region 222 is formed and the window of the oxide film 291 is widened, polycrystalline silicon 251 is deposited and arsenic is ion-implanted for doping the emitter. Polycrystalline silicon 251 is then etched in such a manner as to cover the window. In Fig. 8D, the surface stabilization film 292 is deposited and then annealing is carried out so as to activate the implanted ions and to shallowly diffuse arsenic in polycrystalline silicon into the base layer 221. On the surface layer is formed a diffusion layer including $Si_{1-x}Ge_x$:C containing carbon (C) at this time. Finally, the predetermined regions 211 of the oxide film 291 for inter-level insulation and surface stabilization film 292 are opened and the emitter electrode 252 is formed on polycrystalline silicon 251. Furthermore, the base electrode 26 is formed on the external base extension region 222 and the collector electrode 27, on the collector plug 233.

Figs. 9A-9D show a structure of the bipolar transistor as still different modification of the embodiment shown in Figs. 4A-4B and its fabrication process. The bipolar transistor according to this modification is featured in that boron (B) and nitrogen (N) are doped into the surfaces of the emitter region 21 and silicon-germanium alloy ($Si_{1-x}Ge_1$) region 24. The crystal strain resulting from the lattice mismatch between silicon and germanium is mitigated by introducing B and N having a smaller

lattic constant than silicon, so that the density of the misfit dislocation occurring in the surface layer of the silicon-germanium alloy ($Si_{1-x}Ge_x$) is reduced and the electrical characteristics at the junction between polycrystalline silicon 251 and the emitter region 21 can be improved.

In Fig. 9A, the n^+-buried layer 231 and the n^--collector layer 232 are formed on the Si substrate 20, and the field oxide film 28 is formed on field regions of the bipolar transistor. The p-base layer 221 is formed on one of the sides and the n^+-collector plug 233, on the other. In Fig. 9B, after the oxide film 291 is formed and its predetermined region is opened, germanium is ion-implanted. Furthermore, B and N for mitigating the crystal strain are ion-implanted. In Fig. 9C, the external base extension region 222 is formed and after the window of the oxide film 291 is widened, polycrystalline silicon 251 is deposited and arsenic for doping the emitter is ion-implanted. Polycrystalline silicon 251 is etched in such a manner as to cover the window. In Fig. 9D, after the surface stabilization film 292 is deposited, annealing is carried out in order to activate the implanted ions and to shallowly diffuse arsenic in polycrystalline silicon into the base layer 221. On the surface layer is formed the diffusion layer 211 including $Si_{1-x}Ge_x$: BN containing B and N at this time. Finally, the predetermined regions of the oxide film 291 for inter-level insulation and the surface stabilization film 292 are opened, and the emitter electrode 252 is formed on polycrystalline silicon 251. furthermore, the base electrode 26 is formed on the external base extension region 222 and the collector electrode 27, on the collector plug 233.

Figs. 10A-10D show a bipolar transistor as still another modification of the embodiment shown in Figs. 4A-4B and its fabrication process. The bipolar transistor according to this modification is featured in that carbon (C) is doped into the surfaces of the emitter region and silicon-germanium alloy ($Si_{1-x}Ge_x$) region. The crystal strain resulting from the lattice mismatch between silicon and germanium is mitigated by doping carbon (C) having a smaller lattice constant than silicon, so that the density of the misfit dislocation occurring in the surface layer of the silicon-germanium alloy ($Si_{1-x}Ge_x$) is reduced and the electrical characteristics at the junction between polycrystalline silicon 251 and the emitter region 21 can be improved. Furthermore, due to the decrease of the misfit dislocation of the surface layer, the base-emitter junction is not much affected adversely by the misfit dislocation even when the areas of the emitter region and silicon-germanium alloy ($Si_{1-x}Ge_x$) on the surface side are made equal to each other. Therefore, their areas are made to be equal in this embodiment. As a result, the step of widening the window of the emitter can be omitted and the fabrication process can be simplified.

In Fig. 10A, the n^+-buried layer 231 and the n^--collector layer 232 are formed on the Si substrate 20, and the field oxide film 291 is formed on the field regions of the bipolar transistor. The p-base layer 221 is formed on one of the sides and the N^+ collector plug 233, on the other side. In Fig. 20B, the oxide film 291 is formed and its predetermined regions are opened. Germanium ion is then ion implanted. In Fig. 10C, after the external base extension region 222 is formed, polycrystalline silicon 251 is deposited without widening the window of the oxide film 291, and arsenic for doping the emitter and carbon (C) for mitigating the crystal strain are ion-implanted. Polycrystalline silicon 251 is then etched in such a manner as to cover the window. In Fig. 10D, after the surface stabilization film 292 is formed, annealing is carried out in order to activate the implanted ions and to shallowly diffuse arsenic in polycrystalline silicon into the base layer 221. On the surface layer 211 is formed the diffusion layer $Si_{1-x}Ge_x$:C containing carbon (C) at this time. Finally, the predetermined regions of the oxide film 291 for inter-level insulation and the surface stabilization film 292 are opened, and the emitter electrode 252 is formed on polycrystalline silicon 251. Furthermore, the base electrode 26 is formed on the external base extension region 222 and the collector electrode 27 is formed on the collector plug 233.

A greater effect can be expected by the use of two elements of boron (B) and nitrogen (N) having a smaller lattice constant than silicon in place of carbon (C).

Fig. 11A-11D show a structure of the bipolar transistor as still another modification of the embodiment shown in Figs. 4A-4B and its fabrication process. The bipolar transistor according to the modification is featured in that carbon is doped into the surfaces of the emitter region and silicon-germanium alloy ($Si_{1-x}Ge_x$) region. In the same way as in Figs. 3A-3B, 4A-4B, 5A-5D and 6A-6B, the crystal strain resulting from the lattice mismatch between silicon and germanium is mitigated by doping carbon having a smaller lattice constant than silicon, so that the density of the misfit dislocation occurring in the surface layer of the silicon-germanium alloy ($Si_{1-x}Ge_x$) 24 is reduced and the electrical characteristics at the junction between polycrystalline silicon 251 and the emitter region 21 can be improved. However, the difference from Fig. 10A-10D is that the step of doping carbon (C) and the step of forming the emitter region 21 are reversed. According to this arrangement, since germanium (Ge) and carbon (C) can simultaneously be crystallized, crystallinity of the layer made of $Si_{1-x}Ge_x$:C can be improved and the doping effect

of carbon (C) becomes more distinctive. Furthermore, since carbon (C) is doped, the misfit dislocation of the surface layer of the region 24 is markedly reduced and the base-emitter junction is not much affected adversely by the misfit dislocation occurring in the surface even when the areas of the emitter region 21 and silicon-germanium alloy ($Si_{1-x}Ge_x$) region 24 on the surface side are made equal to each other. Therefore, their areas are made to be equal in this modification. As a result, the step of widening the window of the emitter can be omitted and the fabrication process can therefore be simplified.

In Fig. 11A, the n^+-buried layer 231 and the n^--collector layer 232 are formed on the Si substrate 20, and the field oxide film 28 is formed on field regions of the bipolar transistor. The p-base layer 221 and the n^+-collector plug 233 are formed using the oxide film 28 as the mask. In Fig. 11B, after the oxide film 291 is formed and its predetermined region is opened, germanium is ion implanted. In Fig. 11C, the external base extension region 222 is formed and carbon (C) for mitigating the crystal strain is ion implanted without widening the window of the oxide film 291. Furthermore, annealing is carried out to effect crystallization. On the surface is formed the diffusion layer including $Si_{1-x}Ge_x$:C containing carbon (C) at this time. In Fig. 11D, polycrystalline silicon 251 is deposited and arsenic for doping the emitter is ion implanted. Polycrystalline silicon 251 is etched in such a manner as to cover the window. Furthermore, after the surface stabilization film 292 is deposited, annealing is carried out in order to activate the implanted ions and to shallowly diffuse arsenic in polycrystalline silicon into the base layer 221. Finally, the predetermined regions of the oxide film 291 for inter-level insulation and the surface stabilization film 292 are opened, and the emitter electrode 252 is formed on polycrystalline silicon 251. Furthermore, the base electrode 26 is formed on the external base extension region 222 and the collector electrode 27 is formed on the collector plug 233.

Incidentally, a greater effect can be expected by the use of two elements of boron (B) and nitrogen (N) having a smaller lattice constant than silicon in place of carbon (C).

Embodiment 3:

Fig. 12A-12D show a fabrication process of the bipolar transistor according to still another embodiment.

In Fig. 12A, the n^+-buried layer 231 and the n^--collector layer 232 are formed on the Si substrate 20, and the field oxide film 28 is formed on field regions of the bipolar transistor. The n^+-collector plug 233 is formed using the oxide film 28 as the mask. In Fig. 12B, after the oxide film 290 is formed on the n^--collector layer 232, a photoresist film PF is deposited thereon. Next, a window having a predetermined pattern is formed on the resist film PR and a protective oxide film 290 is etched back using this resist film PR as the mask. Furthermore, the n^--collector layer 232 below this oxide film 290 is etched so as to form a trench into the n^--collector layer 232. In Fig. 12C, after the resist film PR is removed, the silicon-germanium alloy ($Si_{1-x}Ge_x$) is grown selectively and epitaxially in such a manner as to bury the trench by a CVD process and to form the silicon-germanium alloy ($Si_{1-x}Ge_x$) layer 24. After the oxide film 290 is once removed, the p-base layer 221 is formed. In Fig. 12D, the external base extension region 222 is formed and the oxide film 291 is formed once again. After the predetermined region is opened, polycrystalline silicon 251 is deposited, and arsenic is then ion-implanted for doping the emitter. Polycrystalline silicon is etched in such a manner as to cover the window. After the surface stabilization film 292 is deposited, annealing is carried out in order to activate the implanted ions and to shallowly diffuse arsenic in polycrystalline silicon into the base layer 221. Finally, the predetermined regions of the inter-level insulating oxide film 291 and surface stabilization film 292 are opened, and the emitter electrode 252 is formed on polycrystalline silicon 251. Furthermore, the base electrode 26 is formed on the external base extension region 222 and the collector electrode 27, on the collector plug 233.

Embodiment 4:

Figs. 13A-13B show a structure of the bipolar transistor of still another embodiment of the present invention. Fig. 14A is a plan view and Fig. 14B is a sectional view. In comprison with Fig. 3A-3B, the characterizing feature of this embodiment resides in that the base region is formed by self-alignment. Therefore, the principal portions of the bipolar transistor, such as the base region 221, the base electrode extension region 222, etc, can be scaled down. The collector-base junction capacity and the base resistance that impede the switching speed of the bipolar transistor can be reduced with this scale-down.

Figs. 14A-14D show a fabrication process of the bipolar transistor of the Figs. 13A-13B embodiment.

In Fig. 14A, the n^+-buried layer 231 and the n^--collector layer 232 are formed on the Si substrate 20, and the field oxide film 28 is formed on field regions of the bipolar transistor. The n^+-collector plug 233 is formed using the oxide film 28 as

the mask. Similarly, polycrystalline silicon 261 is deposited and oxide film 291 is deposited further thereon. After the predetermined window is formed, the resist film PR is deposited only onto the window of the n^+-collector plug 233 and boron (B) for forming the base layer is ion implanted. In Fig. 14B, a side wall SW1 including an oxide film is formed on the side surface of the window on the base layer 221 and a side wall SW2 including a nitride film is formed on the side wall SW1. Germanium is then ion implanted. In Fig. 14C, after the side wall SW2 including the nitride film is removed, polycrystalline silicon 251 is deposited, and arsenic is ion implanted for doping the emitter region. Thereafter, polycrystalline silicon 251 is etched in such a manner as to cover the window. Thereafter, the base layer 221 and the emitter region 21 are formed in self-alignment by annealing. At this time is formed simultaneously the external extension region 222 of the base region. In Fig. 14D, after the surface stabilization film 292 is deposited, the predetermined regions of the oxide film 291 for interlevel insulation and the surface stabilization film 292 are opened, and the emitter electrode 252 is formed on polycrystalline silicon 251. The base electrode 262 is formed on the external base extension region 222 through polycrystalline silicon 261 and the collector electrode 27 is formed on the collector plug 233.

Embodiment 5:

Figs. 15A-15B show a BiCMOS basic gate (2NAND) circuit to which the bipolar transistor described above is applied. Fig. 15A is a circuit diagram and Fig. 15B shows a sectional structure of a cell. Reference numeral 30 represents the bipolar transistor described above, 31 is a p-channel MOS transistor and 32 is an n-channel MOS transistor. A higher speed circuit operation can be accomplished by using the bipolar transistors described above. Since the bipolar transistor can maintain its high speed performance even at a low power supply voltage, the basic gate circuit operates at a high speed even at a low power supply voltage.

Embodiment 6:

Fig. 16 is a circuit diagram of an ECL (using the output of only the NOR side) gate array to which the bipolar transistors described above are applied. All of the six bipolar transistors are in accordance with the present invention. The ECL circuit is a high speed digital circuit which is constituted by emitter-follower transistors added in order to improve the load driving capacity (load drivability) to a current switch circuit. High speed performance of this circuit can be improved further by employing the bipolar transistors described above. Since the bipolar transistors can maintain their high speed performance even at a low power supply voltage, this basic gate circuit can operate at a high speed even at a low power supply voltage.

Embodiment 7:

Figs. 17A-17B explain a clamp type memory cell to which the bipolar transistor described above is applied. Fig. 17A is a circuit diagram and Fig. 17B shows a sectional structure. Reference numeral 40 in the drawings represents a Schottky barrier diode (SBD) and 41 is a load resistor. The operation speed of the memory cell can much be improved by using the bipolar transistor 42 described above. Since the bipolar transistor can maintain its high speed performance even at a low power supply voltage, the basic gate circuit operates at a high speed even at a low power supply voltage.

Embodiment 8:

Fig. 18 shows a structure of a microprocessor to which the bipolar transistors described above are applied. As is well known, the microprocessor includes a C-cache memory 51 for accepting an instruction, a decoder unit 54, a data structure (DS) microcell 55 for executing an operational processing on the basis of the output signal of the decoder unit and outputting a result, a D-cache memory 52 for storing the result of the operation, a data transistor look-aside buffer (C-TLB) 53a for designating the address for reading out the instruction next to the operation from the cache memory 51, and a D-TLB 53b for converting the logical address of the operation result into a physical address and designating a data storage address.

Microprocessors of the recent years use BiCMOS logic gate circuits for portions which execute the operations, other than memory cells. Therefore, a microprocessor having a higher operation speed can be accomplished by applying the bipolar transistors described above to these portions. Since the bipolar transistor can maintain its high speed performance even at a low power supply voltage, a low power consumption type microprocessor which operates at a high speed even when a power supply voltage drops can be accomplished.

In accordance with the structure according to the present invention the occurrence of the misfit dislocation at the emitter-base junction can be prevented by progressively narrowing the band gap from part of the emitter region side into the base region side. Therefore, the degradation of the elec-

trical characteristics on the hetero-interface, that has been the problem with the prior art, can be eliminated and the higher operation speed of the bipolar transistor can be promoted. The higher operation speed of the bipolar transistor can be promoted, also by the effect of the drift field since the band gap in the base region is changed.

The barrier height of the valence band near the emitter-base junction becomes greater by doping carbon (C) having the function of widening the band gap or boron (B) and nitrogen (N) having smaller atomic radius than silicon (Si) into the emitter region side. As a result, the current gain can be improved and the higher operation speed of the bipolar transistor is promoted.

The silicon-germanium alloy ($Si_{1-x}Ge_x$) having a dimension substantially equal to, or below, that of the emitter region is disposed immediately below and inside the emitter region and in consequence, the silicon-germanium alloy ($Si_{1-x}Ge_x$) is localized. As a result, the density of the misfit dislocation due to the lattice mismatch can be reduced and the influences of the misfit dislocation on the electrical characteristics of the bipolar transistor can be mitigated.

The area of the emitter region on the substrate surface is made greater than the area of the silicon-germanium alloy ($Si_{1-x}Ge_x$) region, so that the emitter-base junction can be spaced apart from the misfit dislocation occurring on the surface of the silicon-germanium alloy ($Si_{1-x}Ge_x$) region and the degradation of the electrical characteristics of the bipolar transistor due to the misfit dislocation can be suppressed.

Since carbon (C) is an element of the same Group IV as silicon and germanium and is electrically intrinsic and since it has a smaller lattice constant than silicon, doping of carbon (C) into the substrate surface mitigates the strain resulting from the lattice mismatch between silicon and germanium and can suppress the occurrence of the misfit dislocation that will otherwise occur on the surface of the silicon-germanium alloy region.

Two elements having ion bondability (such as boron (B) and nitrogen (N)) make re-construction of the silicon-germanium alloy much more easier than the covalence bondable element having a high bonding power, i.e. carbon (C). Therefore, doping of the two elements having a smaller lattice constant than silicon into the substrate surface provides a greater suppression effect of the misfit dislocation than doping of carbon.

In the silicon-germanium base lateral heterojunction bipolar transistor, widening of the width of the substrate surface layer of the base region spaces apart the emitter-base junction and the base-collector junction away from the misfit dislocation, suppresses the occurrence of any excessive current at the emitter-base junction, and reduces the occurrence of the leakag current at the base-collector junction.

Claims

1. A bipolar transistor including a collector region (13, 23) formed of a semiconductor having one conductivity type, a base region (12, 22) formed of a semiconductor having the other conductivity type and a base-collector junction formed between the base region and said collector region (13, 23) in the proximity of said collector region (13, 23), and an emitter region (11, 21) formed of a semiconductor having one conductivity type and an emitter-base junction formed between said emitter region and said base region (12, 22) in the proximity of said base region (12, 22), wherein an energy band gap of said emitter region (11, 21) and said base region (12, 22) near said base-emitter junction is narrowing along a direction of from said emitter region (11, 21) to said base region (12, 22).

2. A bipolar transistor including a collector region (13, 23) formed of silicon having one conductivity type, a base region (12, 22) formed of silicon having the other conductivity type and a collector-base junction formed between the base region and said collector region (13, 23) in the proximity of said collector region (13, 23), and an emitter region (11, 21) formed of silicon of one conductivity type and a base-emitter junction formed between the emitter region and said base region (12, 22) in the proximity of said base region (12, 22), wherein germanium exists in mixture in said emitter region (11, 21) and in said base region (12, 22) near said base-emitter junction, and the concentration of the germanium is increasing along a direction of from said emitter region (11, 21) to said base region (12, 22).

3. A bipolar transistor including a collector region (13, 23) of one conductivity type, a base region (12, 22) of the other conductivity type and a collector-base junction formed between said base region and said collector region (13, 23) in the proximity of said collector region (13, 23), and an emitter region (11, 21) of one conductivity type and a base-emitter junction formed between the emitter region and said base region (12, 22) in the proximity of said base region (12, 22), wherein said emitter region (11, 21) and said base region (12, 22) are formed of a silicon-germanium alloy, and the concentration of germanium is increasing in

the proximity of said base-emitter junction along a direction of from said emitter region (11, 21) to said base region (12, 22).

4. A bipolar transistor according to Claim 3, wherein at least one element having a smaller lattice constant than silicon is contained in an area of from the surface of said emitter region (11, 21) to said base region (12, 22).

5. A bipolar transistor comprising a collector region (13, 23) having one conductivity type, a base region (12, 22) having the other conductivity type and a collector-base junction formed between said base region and said collector region (13, 23) in the proximity of said collector region (13, 23), and an emitter region (11, 21) having one conductivity type and a base-emitter junction formed between said emitter region and said base region (12, 22) in such a manner as to extend from the surface of said base region (12, 22) into said emitter region (11, 21), wherein a portion of said emitter region (11, 21) other than its peripheral portion and a portion of said base region (12, 22) adjacent thereto are formed of a silicon-germanium alloy, the rest of the portions of said emitter region (11, 21) and said base region (12, 22) are formed of silicon, and a germanium concentration in said alloy portion is increasing in a direction extending from said emitter region (11, 21) to said base region (12, 22).

6. A bipolar transistor according to Claim 5, wherein the portion of said collector region (13, 23) adjacent to said alloy portion of said base region (12, 22) is formed of a silicon-germanium alloy.

7. A bipolar transistor according to Claim 5 or Claim 6, wherein at least one element having a smaller lattice constant than silicon is contained in an area of from the surface of said emitter region (11, 21) said base region (12, 22).

8. A bipolar transistor according to Claim 7, wherein said element having a smaller lattice constant than silicon is at least one element selected from the group essentially consisting of carbon, boron and nitrogen.

9. A bipolar transistor comprising a collector region (13, 23) formed of silicon having one conductivity type, a base region (12, 22) formed of silicon having the other conductivity type and a collector-base junction formed between said base region and said collector region (13, 23) in the proximity of said collector region (13, 23), and an emitter region (11, 21) formed of silicon having one conductivity type and a base-emitter junction formed between said emitter region and said base region (12, 22) in such a manner as to extend from the surface of said base region (12, 22) into the inside, wherein germanium exists in mixture in said emitter region (11, 21) and in said base region (12, 22) near the portion spaced apart from an exposed end of said base-emitter junction, and a germanium concentration is increasing in a direction of from said emitter region (11, 21) towards said base region (12, 22).

10. A bipolar transistor according to Claim 9, wherein at least one element having a smaller lattice constant than silicon is contained in an area of from the surface of said emitter region (11, 21) into said base region (12, 22).

11. A method of fabricating a bipolar transistor comprising the steps of:

preparing a silicon substrate (20) having a first region (13, 23) of one conductivity type, a second region (12, 22) having the other conductivity type and a lower impurity concentration than said first region and a third region (11, 21) having the other conductivity type and a higher impurity concentration than said second region, in order named from the side of one of main planes of said substrate (20);

forming a mask having a first window on said one main plane of said silicon substrate (20), and injecting germanium into at least said first region from said first window of said mask so as to form a silicon - germanium alloy region (24) the germanium concentration of which progressively increases away from said one plane inside said first region (13, 23); and

widening said first window on said one main plane of said silicon substrate (20) into a second window greater than said first window, and then injecting an impurity exhibiting the first conductivity type from said second window into said first region so that a p-n junction defined with said first region forms a fourth region of one conductivity type positioned at said silicon - germanium alloy region (24).

12. A method of fabricating a bipolar transistor according to Claim 11, wherein said silicon - germanium alloy region (24) extends from the surface of said first region (13, 23) into said second region (12, 22) in said mask forming and germanium injecting step.

13. A method of fabricating a bipolar transistor according to Claim 11 or Claim 12, wherein at least an element having a smaller lattice constant than that of silicon is injected from said first window of said mask into at least said first region (13, 23).

14. A method of fabricating a bipolar transistor comprising the steps of:

preparing a silicon substrate (20) having a first region (13, 23) of one conductivity type, a second region (12, 22) having the other conductivity type and a lower impurity concentration than said first region and a third region (11, 21) having the other conductivity type and a higher impurity concentration than said second region, in order named from the side of one of main planes of said silicon substrate (20);

forming a mask having a window on said one plane of said silicon substrate (20), and injecting germanium into at least said first region (13, 23) from said window of said mask so as to form a silicon - germanium alloy region (24) the germanium concentration of which is increasing away from said one main plane inside said first region (13, 23); and

injecting an impurity exhibiting one conductivity type from said window of said mask on said one main plane of said silicon substrate (20) into said first region (13, 23) so that a p-n junction defined with said first region forms a fourth region of one conductivity type positioned at said silicon - germanium alloy region (24).

15. A method of fabricating a bipolar transistor according to Claim 14, wherein said silicon - germanium alloy region (24) extends from the surface of said first region (13, 23) into said second region (12, 22) in said mask forming and germanium injecting step.

16. A method of fabricating a bipolar transistor according to Claim 14 or Claim 15, wherein an element having a smaller lattice constant than that of silicon is injected from said window of said mask into at least said first region (13, 23).

FIG. 1A

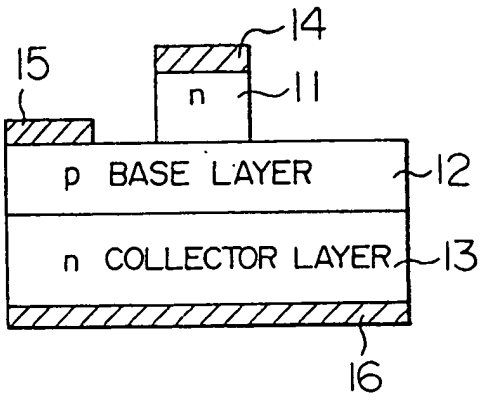


FIG. 1B

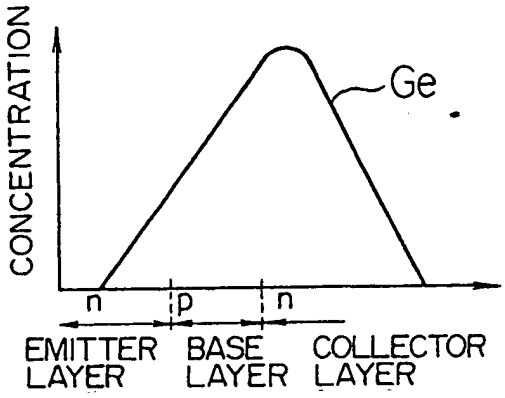


FIG. 1C

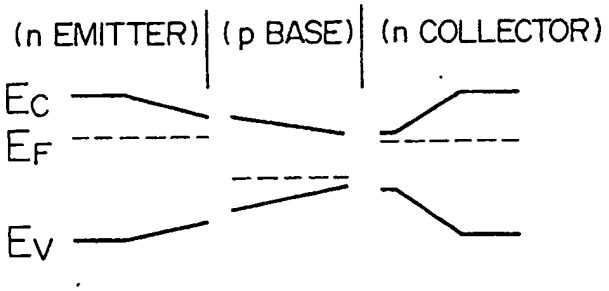


FIG. 1D

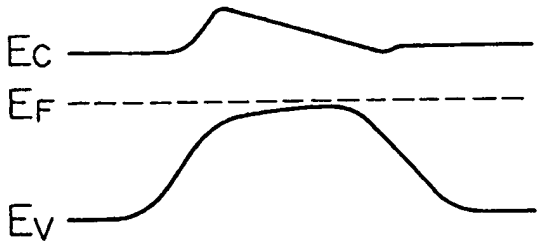


FIG. 1E

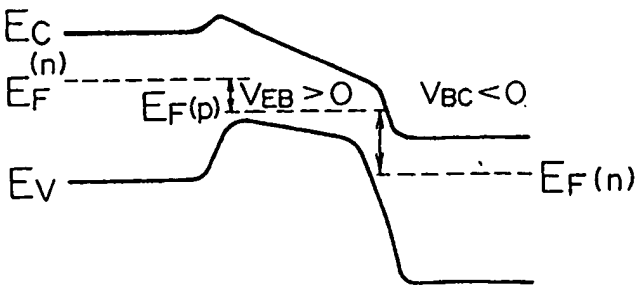


FIG. 2A

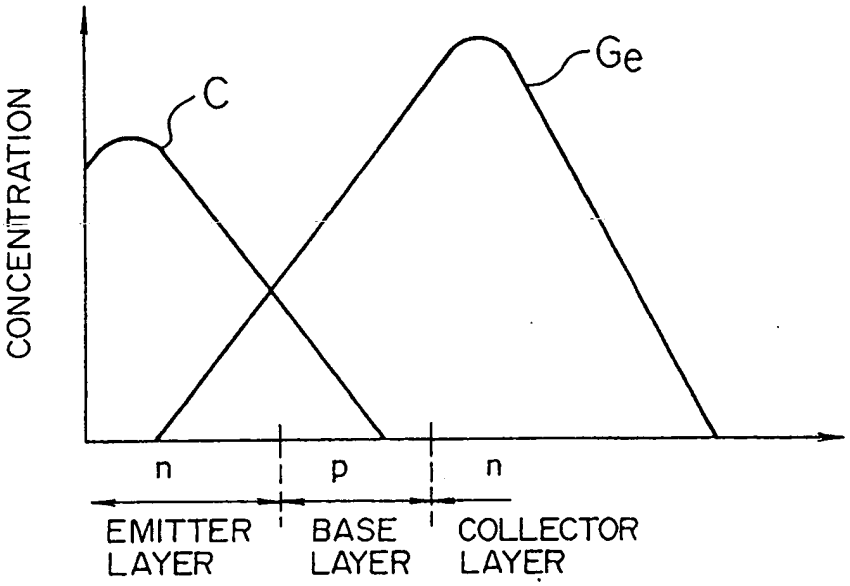

CONCENTRATION
C
Ge
n
p
n
EMITTER LAYER
BASE LAYER
COLLECTOR LAYER

FIG. 2B

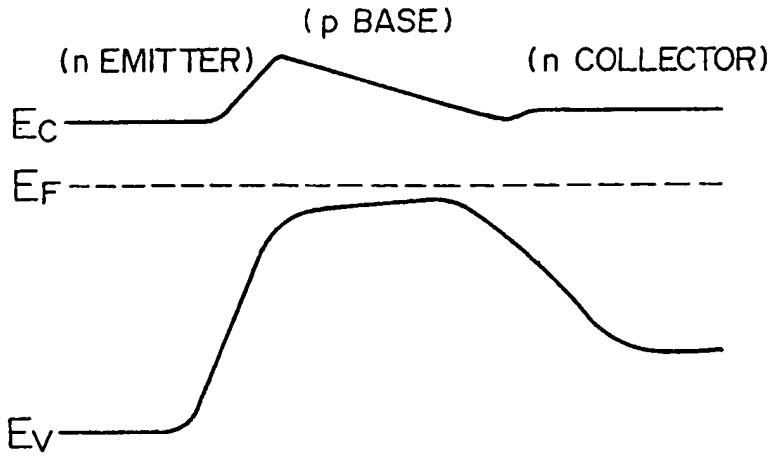

(p BASE)
(n EMITTER)
(n COLLECTOR)
Ec
EF
Ev

FIG. 3A

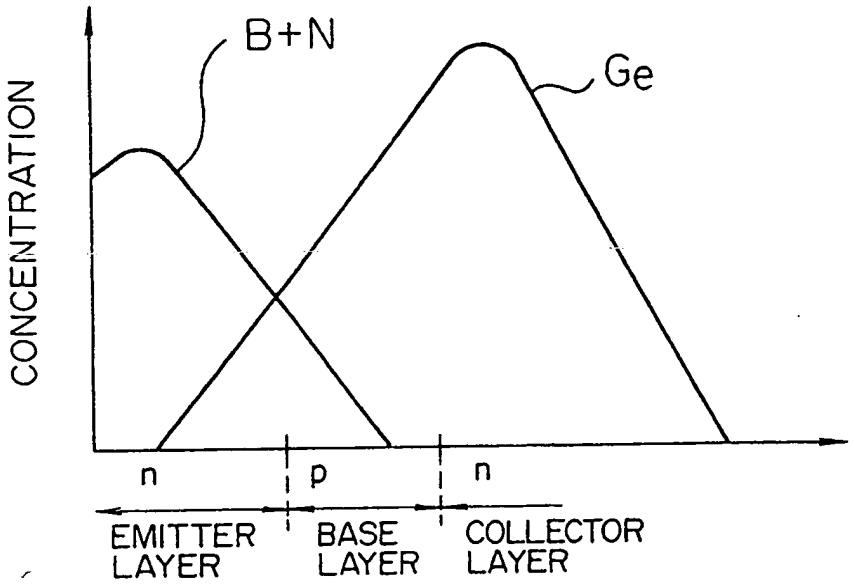

B+N
Ge
CONCENTRATION
n
p
n
EMITTER LAYER
BASE LAYER
COLLECTOR LAYER

FIG. 3B

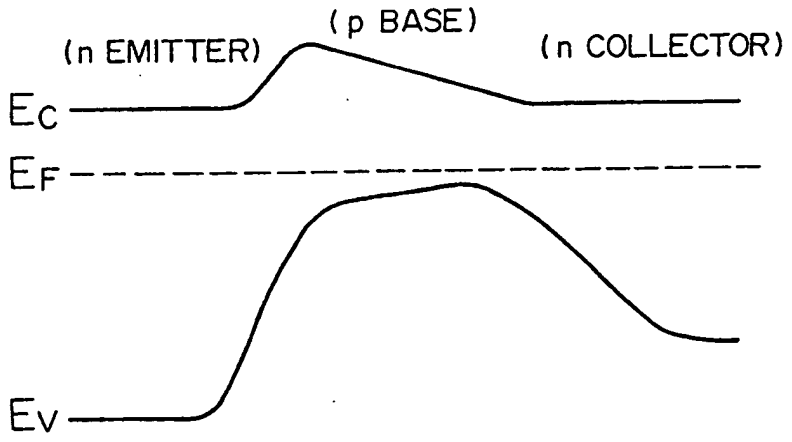

(n EMITTER)
(p BASE)
(n COLLECTOR)
Ec
EF
Ev

FIG. 4A

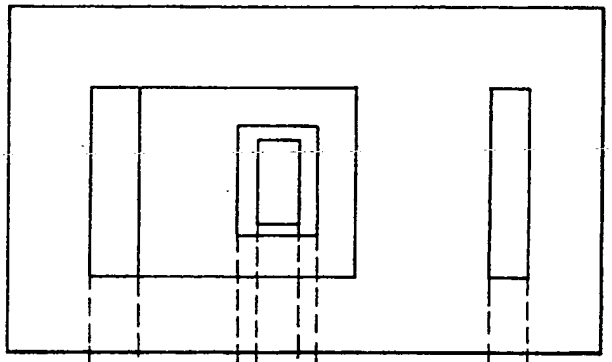


FIG. 4B

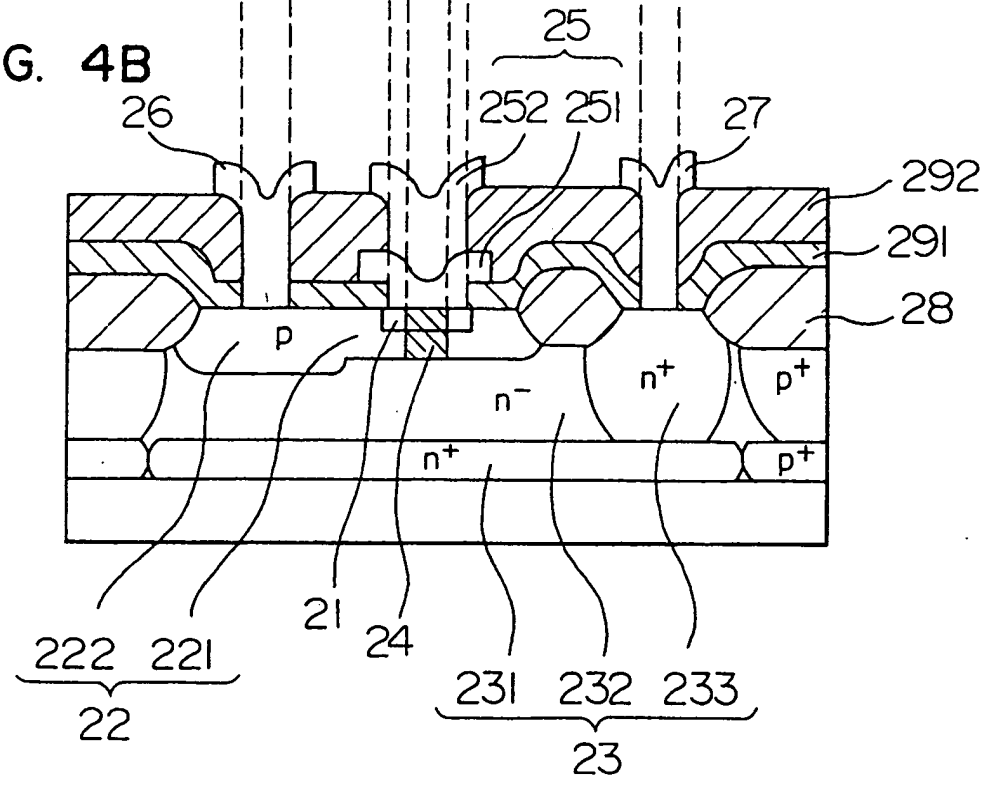


FIG. 5A

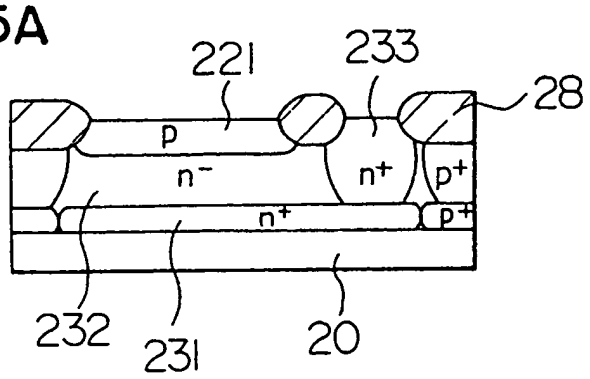


FIG. 5B

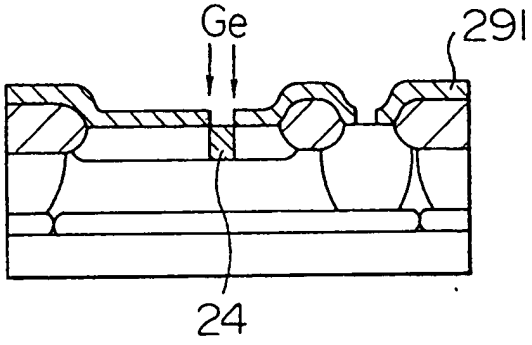


FIG. 5C

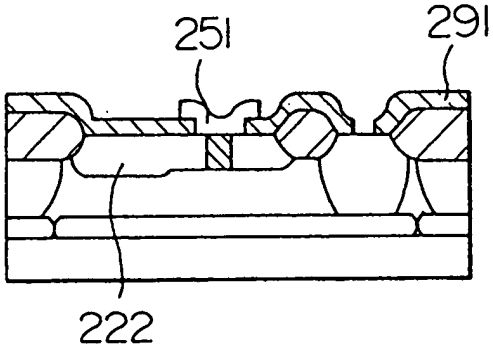


FIG. 5D

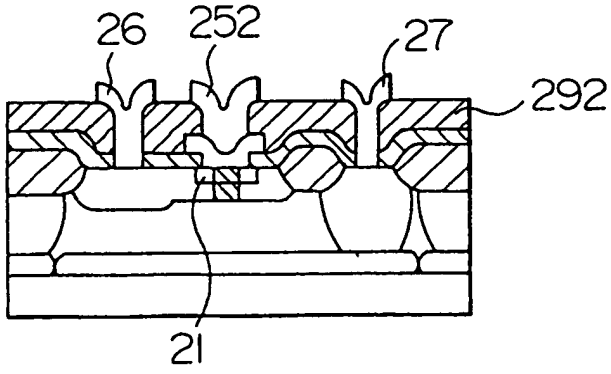


FIG. 6A

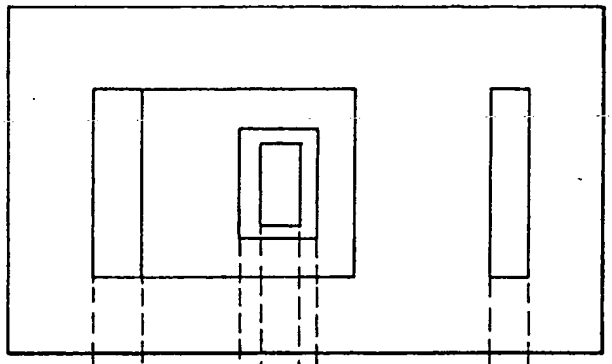


FIG. 6B

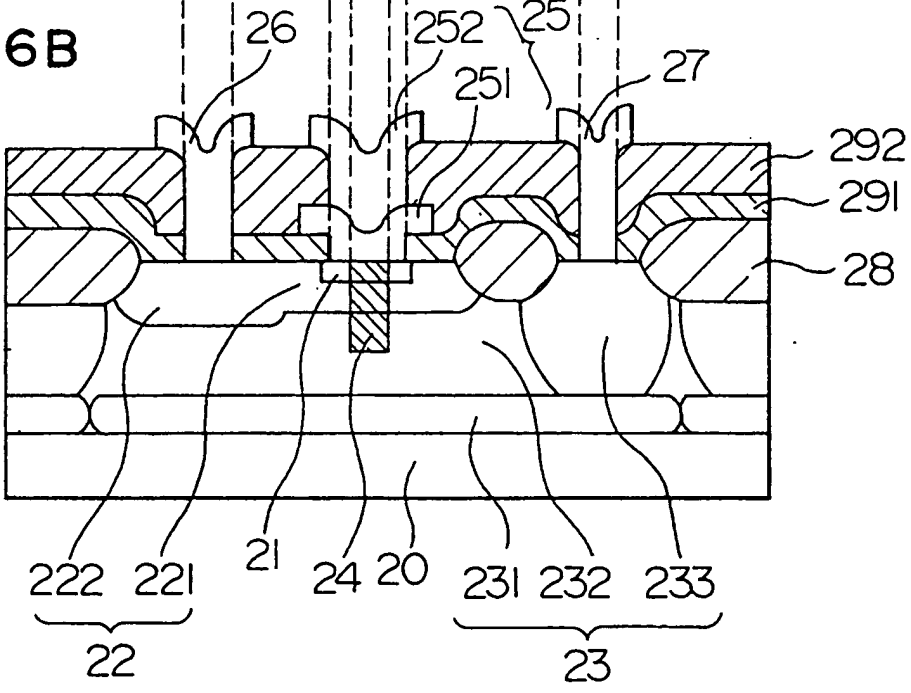


FIG. 7A

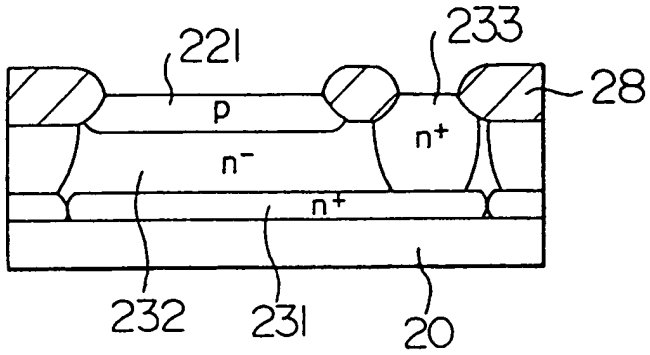


FIG. 7B

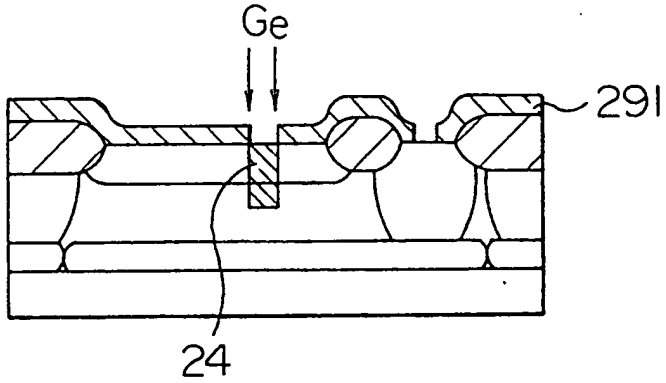


FIG. 7C

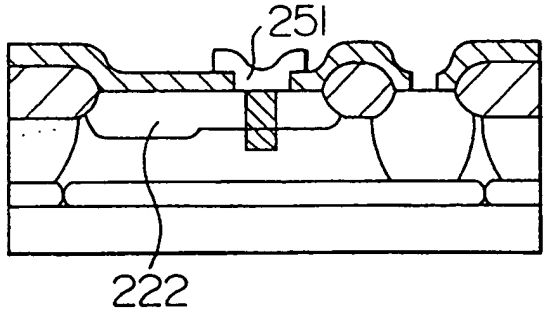


FIG. 7D

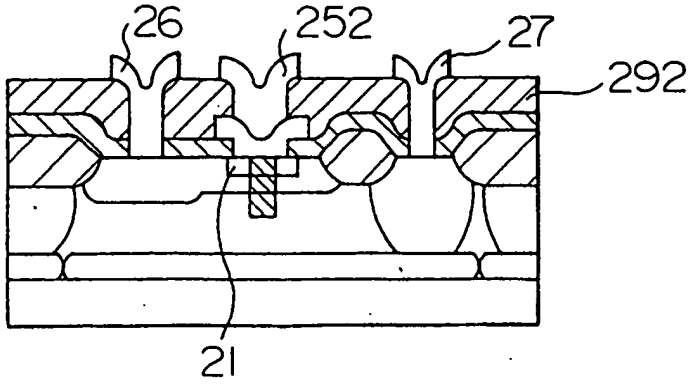


FIG. 8A

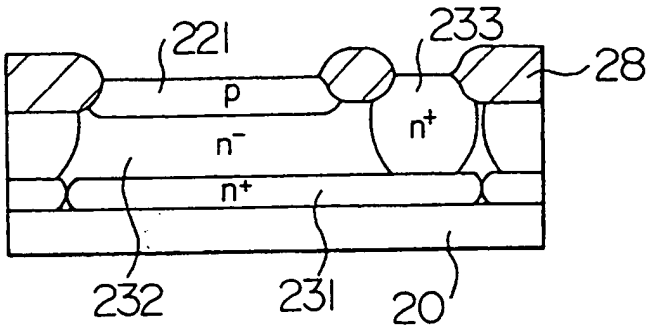


FIG. 8B

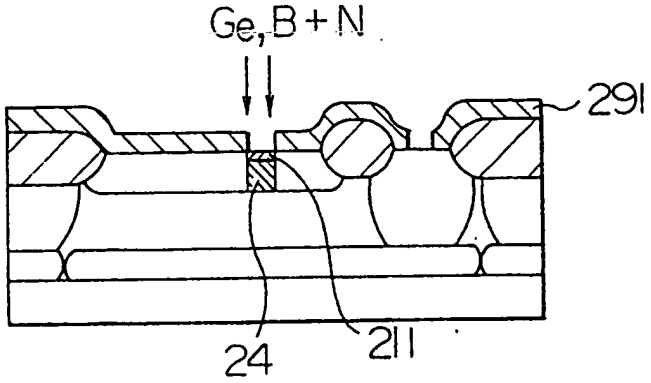


FIG. 8C

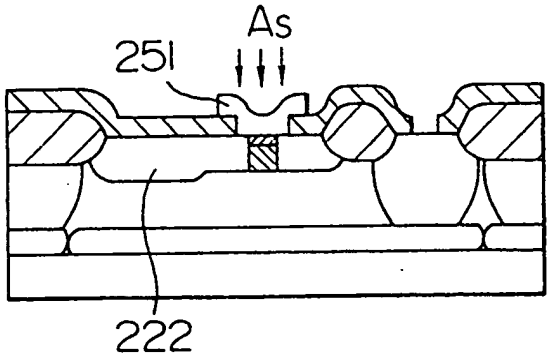


FIG. 8D

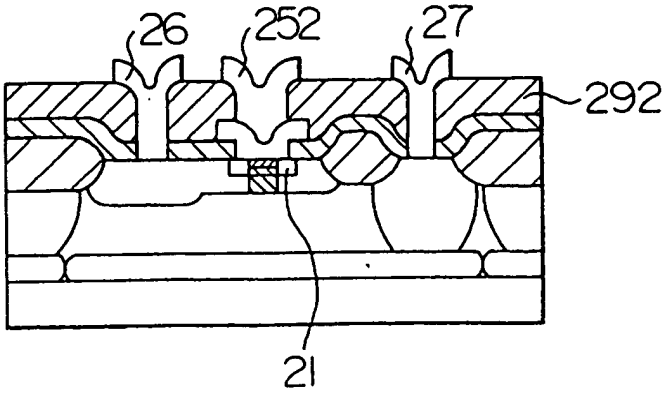


FIG. 9A

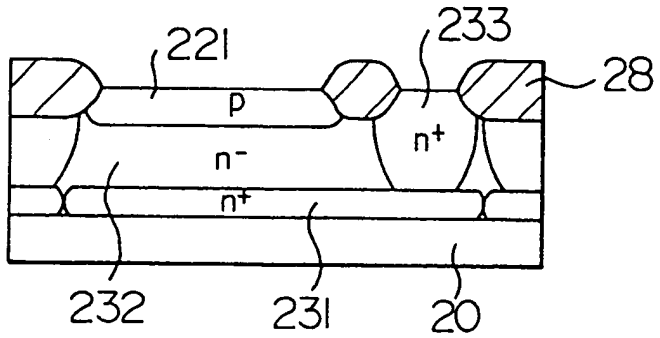


FIG. 9B

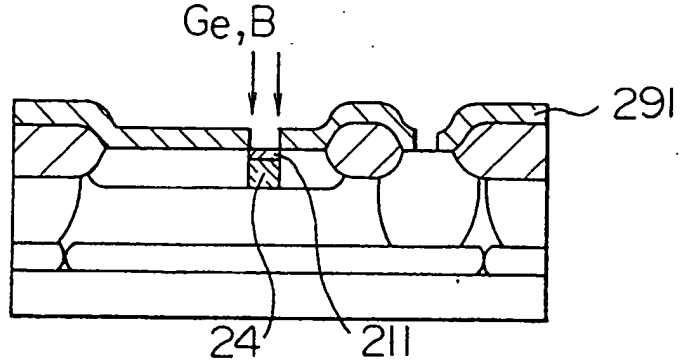


FIG. 9C

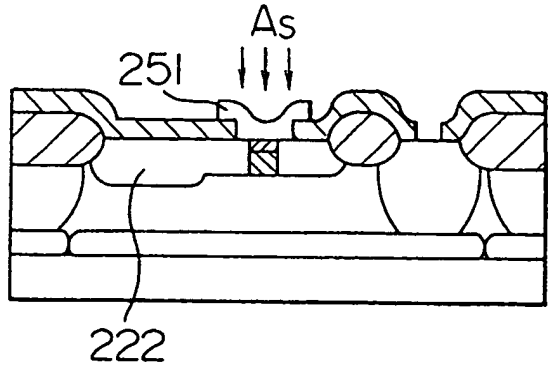


FIG. 9D

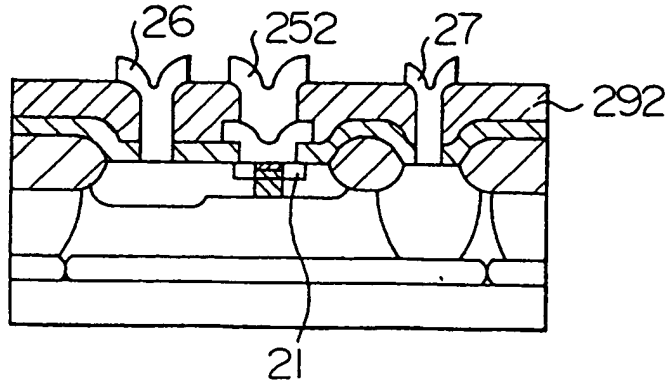


FIG. 10A

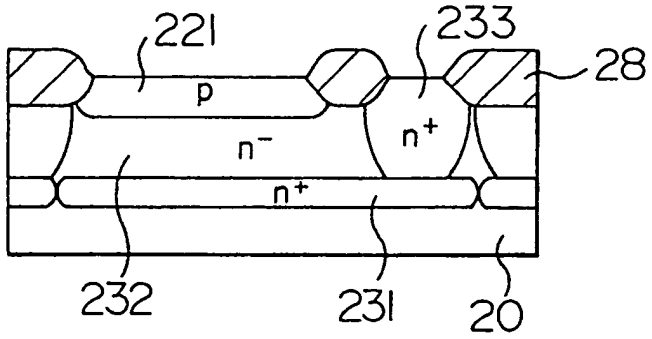


FIG. 10B

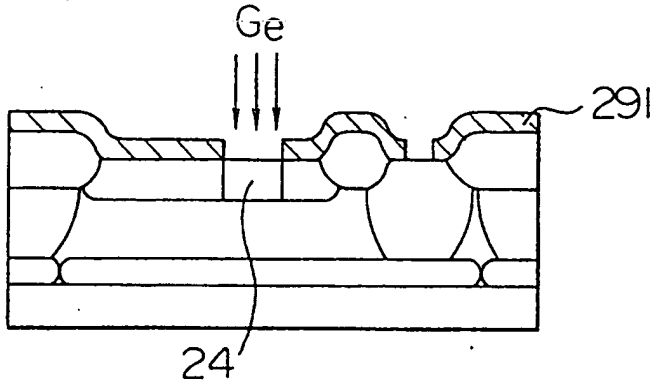


FIG. 10C

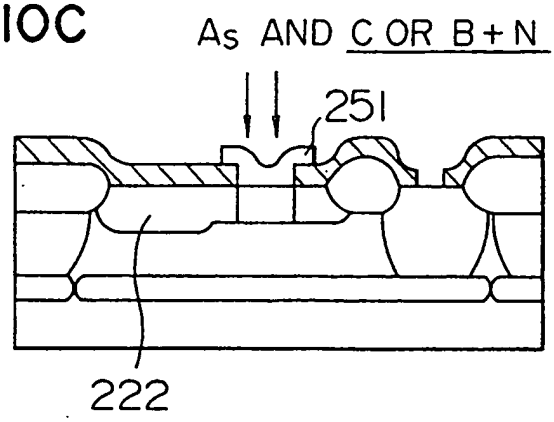


FIG. 10D

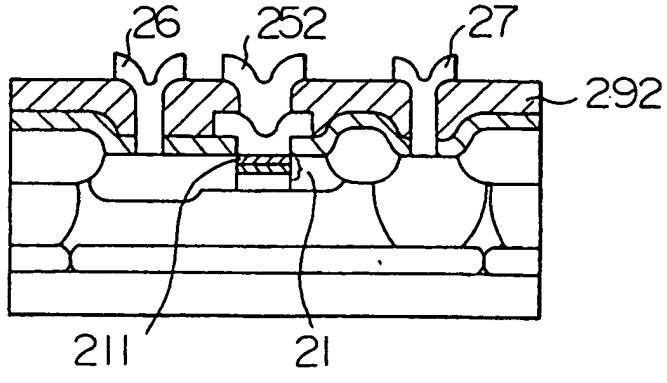


FIG. 11A

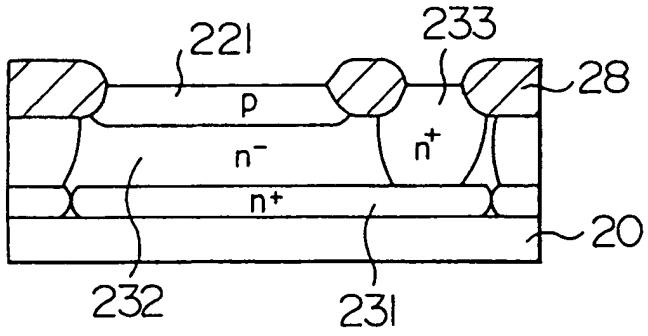


FIG. 11B

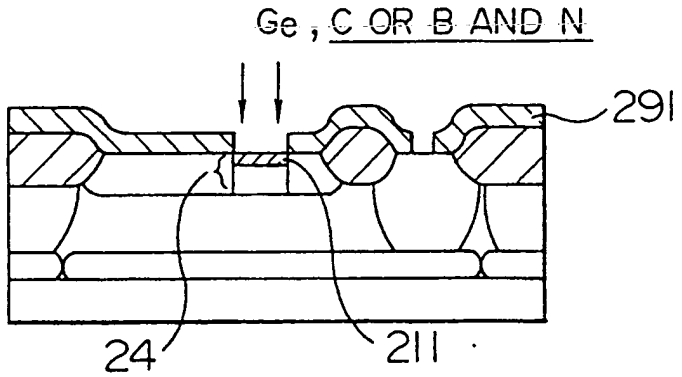


FIG. 11C

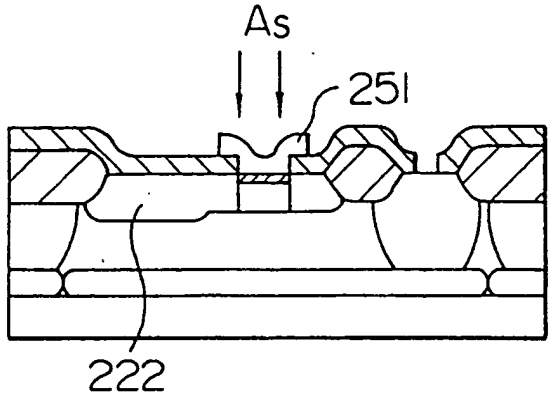


FIG. 11D

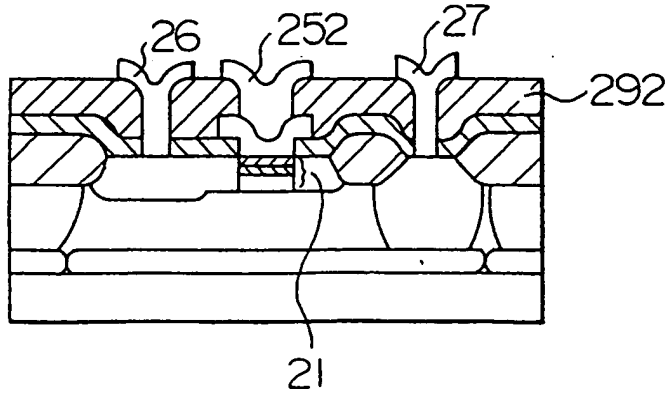


FIG. 12A

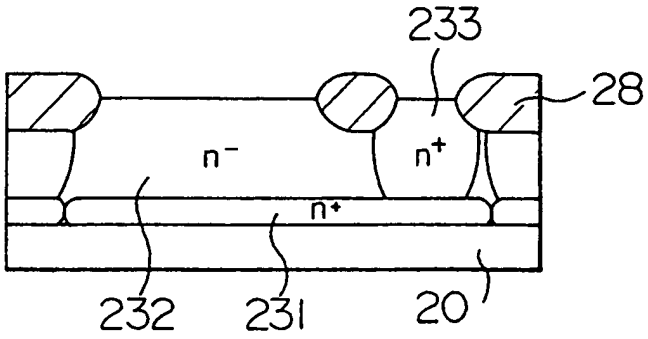


FIG. 12B

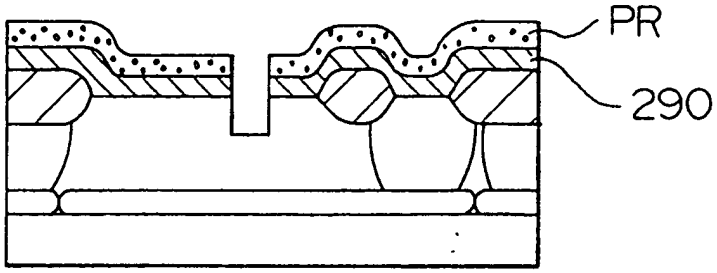


FIG. 12C

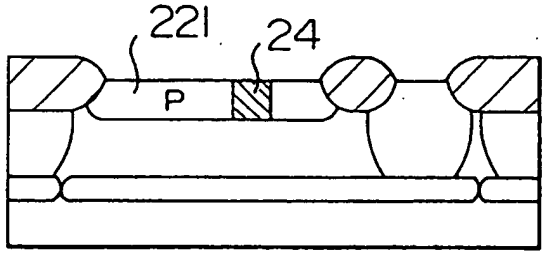


FIG. 12D

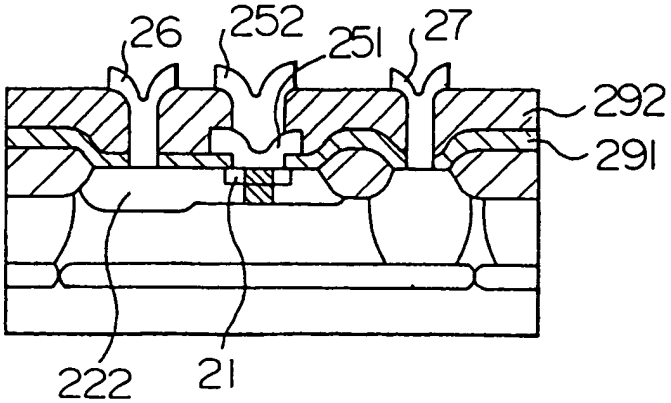


FIG. 13A

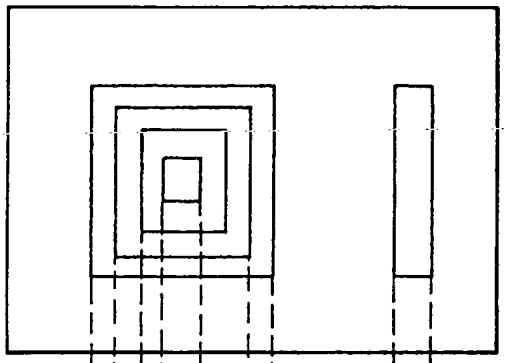


FIG. 13B

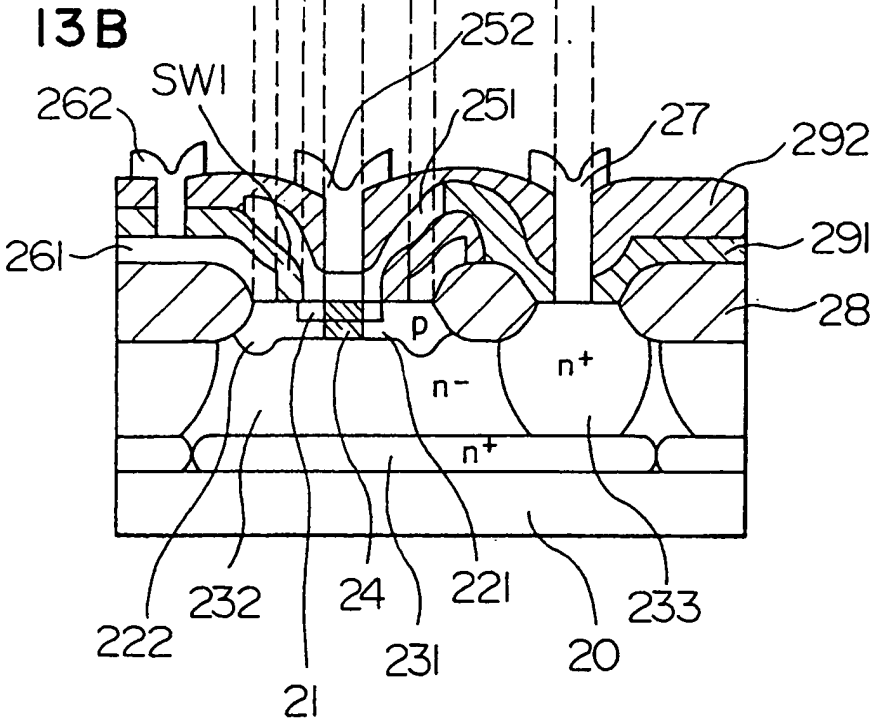


FIG. 14A

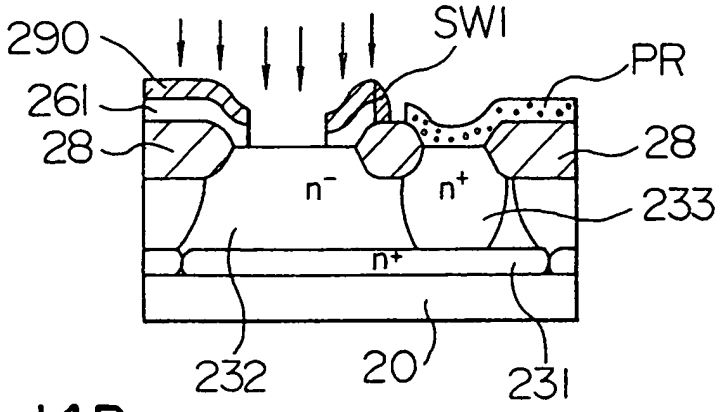


FIG. 14B

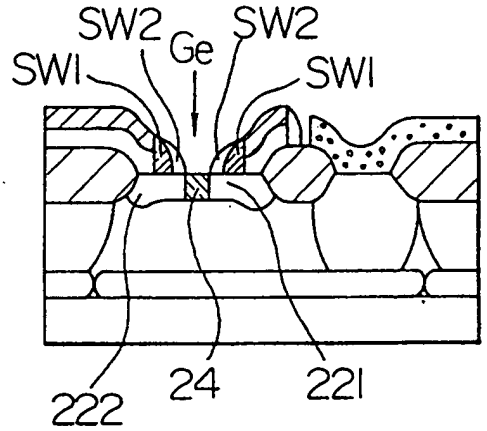


FIG. 14C

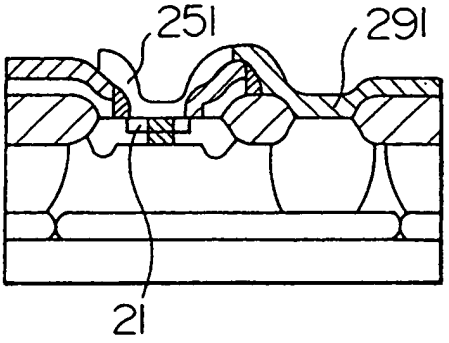


FIG. 14D

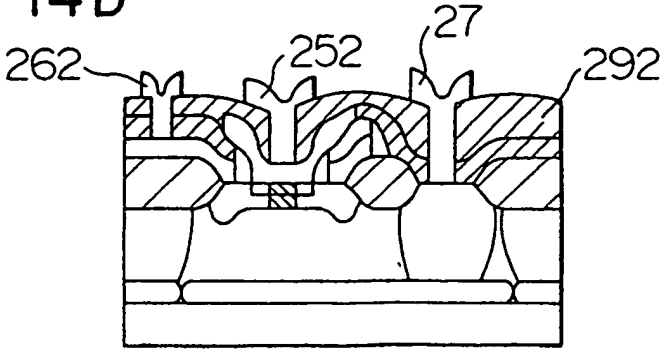


FIG. 15A

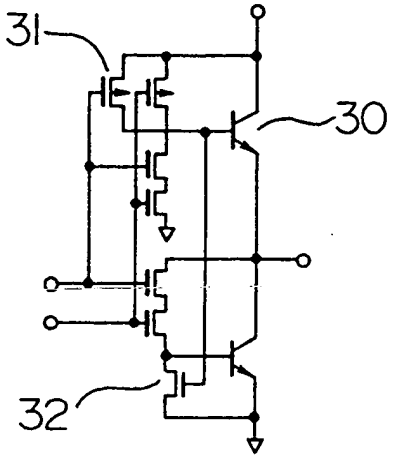


FIG. 15B

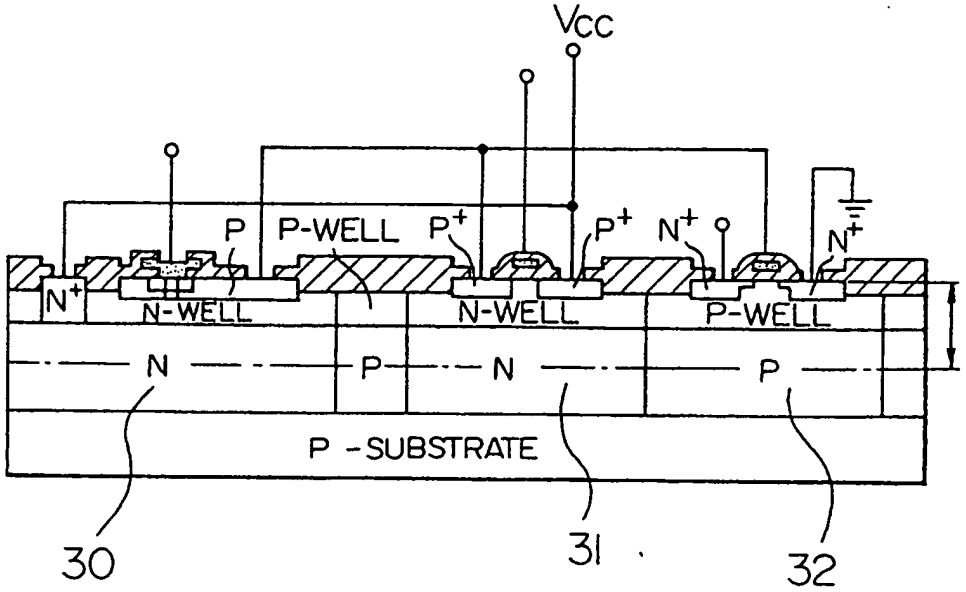


FIG. 16

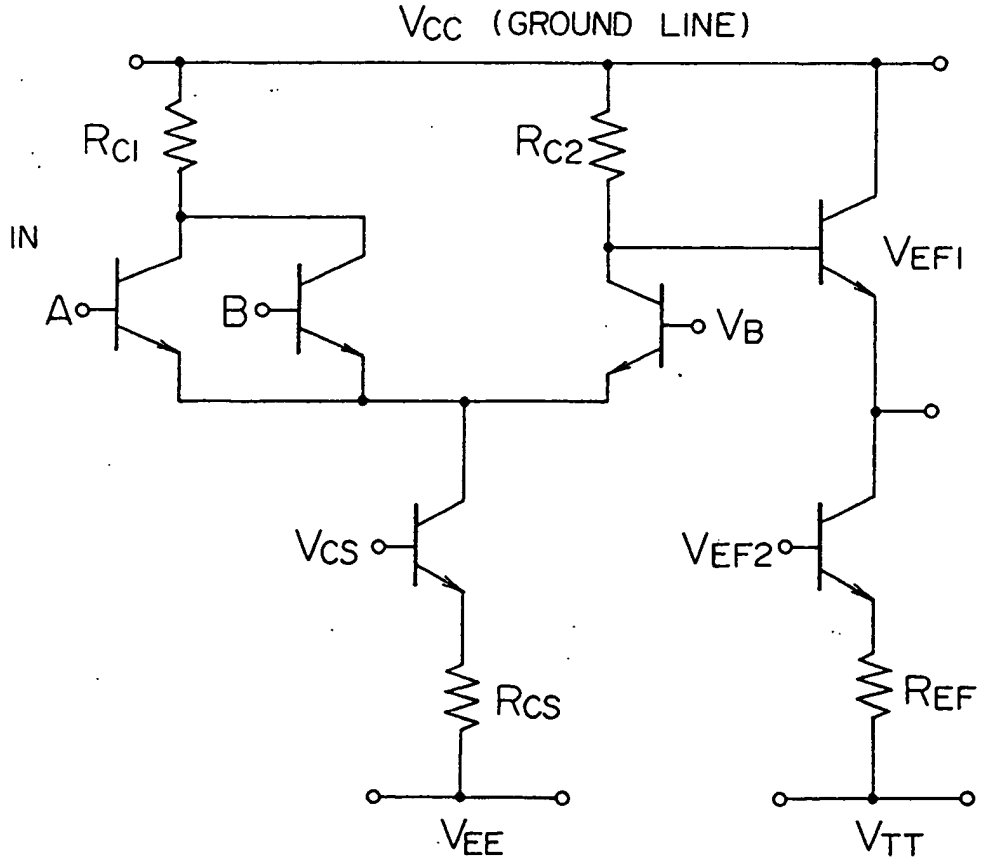


FIG. 17A

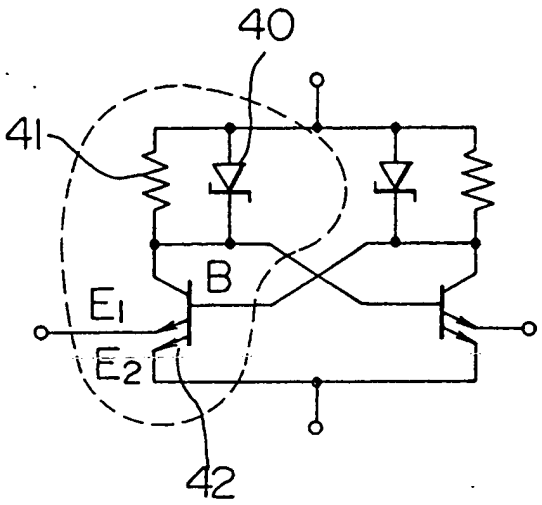


FIG. 17B

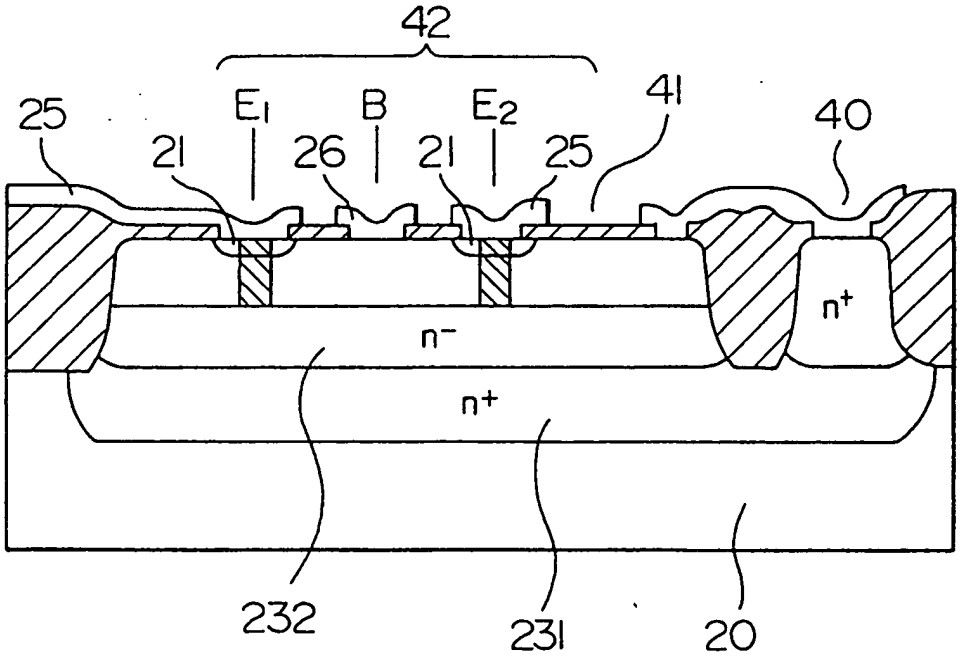


FIG. 18

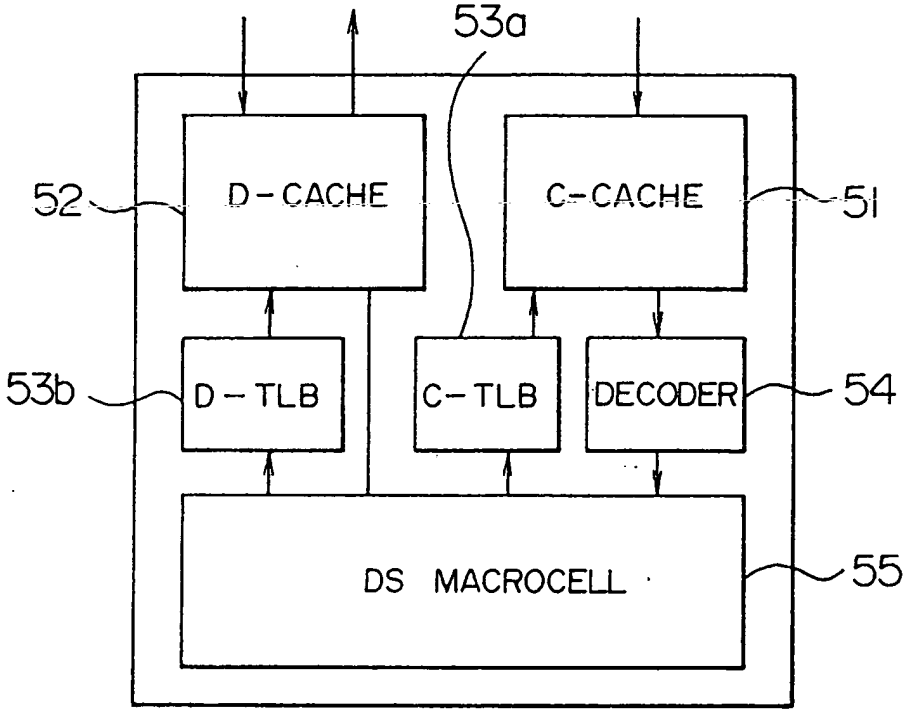
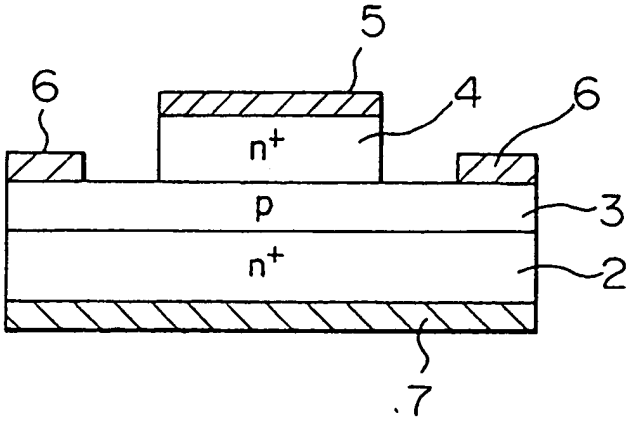

53a
52
D-CACHE
C-CACHE
51
53b
D-TLB
C-TLB
DECODER
54
DS MACROCELL
55

FIG. 19


5
6
4
6
n+
p
3
n+
2
7